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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|-----------------------|------------------|
| 09/288,263 | 04/08/1999 | HIROYUKI WAKI | NAK1-BG55 | 7236 |
| 21611 | 7590 | 08/02/2004 | EXAMINER | |
| SNELL & WILMER LLP 1920 MAIN STREET SUITE 1200 IRVINE, CA 92614-7230 | | | LAFORGIA, CHRISTIAN A | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2131 | 25 |

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/288,263

Applicant(s)

WAKI ET AL.

Examiner

Christian La Forgia

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 30,39-44,52 and 53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 19 April 2004 has been entered.
2. Claims 30, 39-44, 52 and 53 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 30, 39-44, 52, and 53 have been considered but are moot in view of the new ground(s) of rejection.
4. See further rejections that follow.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. As per claims 52 and 53, merely claimed as a computer program representing a computer listing *per se*, that is, descriptions or expressions of such a program and that is, descriptive material *per se*, non-functional descriptive material, and is not statutory because it is not a physical "thing" nor a statutory process, as there are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed aspects of the invention which permit the computer program's functionality to be realized. Since a computer program is merely a set of instructions

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capable of being executed by a computer, the program itself is not a process, without the computer-readable medium needed to realize the computer program's functionality. In contrast, a claimed computer-readable medium encoded with a computer program defines structural and functional interrelationships between the computer program and the medium which permit the computer program's functionality to be realized, and is thus statutory. **Warmerdam**, 33 F.3d at 1361, 31 USPQ2d at 1760. **In re Sarkar**, 588 F.2d 1330, 1333, 200 USPQ 132, 137 (CCPA 1978). See MPEP § 2106(IV)(B)(1)(a).

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 30, 39-44, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Java!**, by Tim Ritchey, hereinafter Ritchey, in view of **Compilers: Principles, Techniques, and Tools**, by Alfred V. Aho et al., hereinafter Aho.

9. As per claims 30 and 39, Ritchey teaches a data storage comprising:

generating a virtual machine instruction sequence by compiler to be executed by a virtual machine, see page 53, "Finally, the Javac compiler enables developers to compile for the Java Virtual Machine, providing applications which will run on any system for which the browser or interpreter have been ported," page 326, "The Java system begins with the Java code developed by a programmer. This code is fed to a compiler which generates the Java bytecode for the virtual machine", see page 328, "It is the Java Virtual Machine for which the Java compiler compiles the source code";

transmitting the instruction block to the virtual machine, see page 331, Figure 14.1;

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storing the instruction block in the virtual machine, see pages 336-342, specifically Sections entitled “The Instruction Set,” “The Registers,” “The Java Stack,” “Local Variables,” “Execution Environment,” “Operand Stack,” and “The Memory Area.”

10. For a better illustration of a java compiler and transmitting the instruction block to the virtual machine please refer to pages 162 and 163, specifically Figures 9.1 and 9.2, of **Java Developer’s Reference**, by Mike Cohn et al.

11. Ritchey does not teach dividing the virtual machine instruction sequence into basic blocks each corresponding to an instruction block, see pages 336-337, “The instruction set for the JVM [Java Virtual Machine] is exactly equivalent to the instruction set for a CPU,” for dividing the virtual machine instruction sequence into sets corresponding to instruction sets for a CPU.

12. Aho discloses dividing the machine instruction sequence into basic blocks each corresponding to an instruction block, see pages 529-530, Algorithm 9.1, Example 9.2, and Figures 9.7 and 9.8.

13. Aho defines a basic block as a sequence of consecutive statements in which flow of control enters at the beginning and leaves at the end without halt or possibility of branching except at the end. Therefore, Aho teaches wherein the format of the instruction block includes an identifier area for storing an identifier that specifies a start position of the instruction block, see page 529, Aho’s discussion of determining of *leaders*. According to Aho’s definition provided above, the next part of the basic block would be a non-branch instruction area for storing non-branch instructions belonging to the corresponding basic block. Still going by Aho’s definition of a basic block, the branch instruction area would have to be at the end of the basic

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block thereby designating the next leader or basic block. Aho further discloses storing branch identifiers on pages 546-552. This is further based on the definition of a basic block as defined in column 2, lines 15-23 of U.S. Patent No. 6,044,222 to Simons et al., which states:

A basic block is a contiguous sequence of instructions such that control flow can only enter at the first instruction and leave at the last instruction. Basic blocks have the characteristic that if one of the instructions is ever executed by the program, all the instructions in the basic block will be executed (assuming that no exceptions occur). A basic block typically starts at a branch label and is typically terminated by some sort of a branch instruction.

Graphical representations of basic blocks can be found in Figures 1-6, 10, 12, 15-21, 23a, 23b, 23c, 26a, and 28b of U.S. Patent No. 5,923,883 to Tanaka et al.

14. It would have been obvious to one of ordinary skill in the art at the time the invention was made for the compiler to divide the virtual machine instruction sequence into basic blocks each corresponding to an instruction block, since Aho states on page 530, section 9.4 that such a modification would be useful for optimizing the code in an effort to reduce the overall running time or space required for the final program.

15. Regarding claim 40, Ritchey teaches wherein the identifier of the instruction block is address related information in the virtual machine instruction sequence, see page 330.

16. With regards to claim 41, Aho teaches wherein the address related information is one of absolute address, relative address, and offset address, see pages 519 and 520.

17. Regarding claim 42, Ritchey discloses wherein whether each virtual machine instruction is positioned at a start position of the basic block is indicated by an address in the virtual machine instruction sequence to which the virtual machine instruction is allocated, see page 330;

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a virtual machine instruction at the start position of the basic block being allocated to a specific address in the virtual machine instruction sequence, see page 330, and

a virtual machine instruction at other than the start position of the basic block being allocated to an address other than the specific address, see page 330.

18. Regarding claim 43, Ritchey teaches an identifying unit for storing identification information which indicates if the virtual machine instruction is positioned at a start position of the basic block, see page 339, the program counter;

an operation specifying unit for specifying an operation to be executed by the virtual machine, see pages 336-338, "The Instruction Set."

19. Regarding claim 44, Aho teaches the basic blocks, see pages 528-533;

identification tags, each designates an address related information of the virtual machine instruction at a start position of the basic block; attachment of the tag indicating if the virtual machine instruction corresponding to the identification tag is positioned at the start position of the basic block, pages 546-533.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

21. The following patents are cited to further show the state of the art with respect to compilers, such as:

United States Patent No. 5,838,980 to Guillen et al., which is cited to show compilation and virtual machine arrangement and a process for source code including pre-runtime executable language structure constructs.

United States Patent No. 6,021,273 to Griesemer, which is cited to show interpreter generation and implementation utilizing interpreter states and register caching.

United States Patent No. 6,092,147 to Levy et al., which is cited to show a virtual machine with securely distributed bytecode verification.

United States Patent No. 6,151,618 to Wahbe et al., which is cited to show safe general purpose virtual machine computing system.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (703) 305-7704. The examiner can normally be reached on Monday thru Thursday 7-5.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (703) 305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian LaForgia

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Patent Examiner

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clf


AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100